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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	4

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,051	FUJIMORI ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000 and 16 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: NOISE COUNTERMEASURE DETERMINATION METHOD AND APPARATUS AND STORAGE MEDIUM.
2. First named inventor is: FUJIMORI.
3. Claims 1-22 have been submitted, examined, and rejected.
4. Priority is claimed to Japanese patent application 2000-138681 filed May 11, 2000 and also to Japanese patent application 2000-159100 filed May 29, 2000.

Index of Prior Art

5. **Tsuchida** refers to US patent 5,559,997, issued September 24, 1996.
6. **Dorf** refers to The Electrical Engineering Handbook, Second Edition, Richard C. Dorf, CRC Press, 1997, pages 2265-2272.
7. **Guo** refers to US patent 6,597,808, filed December 6, 1999.
8. **Koford** refers to US patent 6,493,658 filed April 19, 1994.

Specification-objections-informalities

9. The Specification is objected to because of the following informalities. Appropriate correction is required.
10. FOREIGN PRIORITY. Specification page 1 claims the priority benefit of two separate Japanese patent applications that were filed on different dates. Specifically, Japanese patent application 2000-138681 filed May 11, 2000 and Japanese patent application 2000-159100 filed May 29, 2000.
11. Claiming the benefit of 2 separate Japanese patent applications does not appear to satisfy 35 USC 119(a) which singularly states "...an application":

> An application for patent for an invention filed in this country by any person who has, or whose legal representatives or assigns have, previously regularly filed **an application for a patent for the same invention in a foreign country** which affords similar privileges in the case of applications filed in the United States or to citizens of the United States, or in a WTO member country, shall have the same effect as the same application would have if filed in this country on the date on which the application for patent for the same invention was first filed in such foreign country, if the application in this country is filed within twelve months from the earliest date

> on which such foreign application was filed; but no patent shall be granted on any application for patent for an invention which had been patented or described in a printed publication in any country more than one year before the date of the actual filing of the application in this country, or which had been in public use or on sale in this country more than one year prior to such filing.

12. Thus, please specify a single Japanese patent application. For the purpose of the present examination, the Examiner will conservatively use priority to the earliest Japanese application date: May 11, 2000.
13. SPECIFICATION. Specification page 13 line 26 states "FIG. 3", apparently should read "FIG. 2."
14. Also, specification page 16 lines 21-23 apparently incorrectly describe the values of components in FIG 5. Specifically, the resistance Rs, and one of the wiring lengths do not match the values in the FIG 5. Please correct either the specification or the figure, so that they are consistent.

35 USC § 112-Second Paragraph-indefinite claims

15. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
16. **Claims 2 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
17. In claim 2, the term **"categorizing the noise"** is not adequately defined. Specifically, the possible categories are not defined.
18. In claim 5, the term "outputting the input circuit information which **includes as, a wiring length, a Manhattan distance which is determined based on positions of part pins forming the target circuit and a wiring topology"** is not adequately defined. Specifically, it is not clear precisely what information is outputted. Possibly the output is a single item (a wiring length), which is equivalent to the Manhattan distance, and the Manhattan distance is determined from the part pins and the wiring topology. See definition of "Manhattan distance" below.

Claim Interpretation

19. **The claim language is interpreted in light of the specification.** Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
20. In claim 1 and throughout the claims, the term **"noise"** is interpreted broadly as any unwanted signals that produce undesired effects, including electric characteristics such as signal delay, electromagnetic radiation, reflection, and cross talk.
21. In claim 4, the term **"ringback"** is interpreted as the "undershoot", per Dorf page 2271 equation (100.27) for transient responses. The oscillations in Dorf FIG 100.6 in response to a step input are commonly known as "ringing".
22. In claim 5, the term "Manhattan distance" is interpreted per Guo at column 6 lines 35-49:

> One technique for assessing distance is to determine whether one end point is within a predetermined radial distance from the other end point. See FIG. 11A. We refer to this as a circular distance function. Another technique is to define a square bounding box of predetermined size around one end point and to determine whether the other end point is within that bounding box. See FIG. 11B. We refer to this as the square distance function. A third technique is to define a square bounding box of predetermined size around one end point and then to rotate the bounding box around that end point to determine if at any rotational orientation the second end point falls within the bounding box. This will occur, if at all, when one corner of the bounding box lies on a line between the two end points. See FIG. 11C. We call this the Manhattan distance function.

Claim Rejections - 35 USC § 102(b)

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country

or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

24. Claim 1-3, 7-12, and 16-22 are rejected under 35 U.S.C. 102(b) as being anticipated.

25. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchida.

26. Claim 1 is an independent method claim with 2 limitations.

27. (a)-**"calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis"** is disclosed by Tsuchida Abstract "noise reduction component addition" and FIG 1 "addition of noise reduction component" and "rated value change" and "all changeable parts".

28. (b)-"comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasure" is disclosed by Tsuchida FIG 1 "addition of noise reduction component" and "rated value change" and "all changeable parts".

29. Claims 2-3 and 7-9 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchida.

30. Claims 2-3 and 7-9 and 20-22 depend directly or indirectly from claim 1.

31. In claim 2: (c)-**"creating a simulation model of the input circuit information after determining the noise countermeasures in said step (b)"** is disclosed by Tsuchida FIG 1 "simulation".

32. (d)-**"carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit to check whether or not a noise exceeding a tolerable range exists in the signal waveform"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation".

33. (e)-**"categorizing the noise existing as a result of the noise check carried out in said step (d), and optimizing the determined noise countermeasures to only portions related to the noise"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component".

34. In claim 3, **"said step (a) outputs a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2**

which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range" is disclosed by Tsuchida FIG 8a-8d, and column 16 line 42 "allowable range... 7V... 5V... then the terminal resistance... 70 to 80Ω."

35. In claim 7: (c)-**"creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures in said step (b)"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component".
36. (d)-**"carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform"** is disclosed by Tsuchida column 2 line 34 and column 16 line 33 "cross talk".
37. (e)-**"categorizing the noise existing as a result of the noise check carried out on said step (d), and optimizing the determined noise countermeasures to only portions of the noise"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component".
38. In claim 8, **"said step (c) creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component" and column 2 lines 31-35 "design rule... cross talk... parallel routes" and column 26 lines 1-10 "design rules... interval 0.1 mm... looks for a design rule according to which the parameter value satisfies a requirement"
39. In claim 9, **"said step (c) and said step (d) are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the**

noise check carried out in said step (d) does not exceed the tolerable range, and said step (b) determines the minimum pattern gap as the noise countermeasures" is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component" and column 2 lines 31-35 "design rule... cross talk... parallel routes" and column 26 lines 1-10 "design rules... interval 0.1 mm... looks for a design rule according to which the parameter value satisfies a requirement"

40. In claim 20, (c)-**"carrying out at least one of a circuit rule check and a wiring topology check with respect to the input circuit information"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component" and column 2 lines 31-35 "design rule... cross talk... parallel routes" and column 26 lines 1-10 "design rules... interval 0.1 mm... looks for a design rule according to which the parameter value satisfies a requirement".
41. In claim 21, (d)-**"outputting an advice based on a check result obtained in said step (c)"** is disclosed by Tsuchida FIG 1 "PC BOARD LAYOUT" and "addition of noise reduction component".
42. In claim 22, **"(e) correcting the input circuit information based on the advice in said step (d)"** is disclosed by Tsuchida FIG 1 "PC BOARD LAYOUT" and "addition of noise reduction component".
43. Claims 10-12 and 16-18 are "apparatus" claims with the same limitations as "method" claims 1-3 and 7-9, and are rejected for the same reasons respectively.
44. Claim 19 is a "computer readable storage media" claim with the same limitations as "method" claim 1, and is rejected for the same reasons

45. Claim Rejections - 35 USC § 103

46. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

47. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.

48. Claims 1-6 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable.

49. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchida in view of Dorf.

50. Tsuchida does not disclose the additional limitation.

51. **"said step (a) compares a damping resistance which makes a voltage at a time of a ringback equal to the minimum voltage VIH-1 and the minimum value of the damping resistance, and outputs a larger one of the damping resistance"** is disclosed by Dorf page 2271 equation (100.27) "undershoot" for transient responses. The oscillations in Dorf FIG 100.6 in response to a step input are commonly known as "ringing" (like ringing a bell).

52. MOTIVATION FOR CLAIM 4. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dorf to modify Tsuchida. One of ordinary skill in the art would have started with Tsuchida column 16 line 24 as disclosing an "allowable range" of voltage for the overshoot, and then looked to Dorf for classical transient response analysis to also keep the undershoot within the allowable range, because a voltage outside of (above or below) the allowable range may cause undesired and/or indefinite results. Note that Tsuchida FIG 8c and 8d each have the first undershoot (or ringback) equal to the minimum voltage of the allowable range. Thus, Tsuchida implicitly teaches towards the importance of staying above the minimum voltage during the undershoot.

53. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchida in view of Guo.

54. Tsuchida does not disclose the additional limitation.

55. (c)-**"outputting the input circuit information which includes as, a wiring length, a Manhattan distance which is determined based on positions of part pins forming the target circuit and a wiring topology"** is disclosed by Guo at column 6 lines 35-49:

> One technique for assessing distance is to determine whether one end point is within a predetermined radial distance from the other end point. See FIG. 11A. We refer to this as a circular distance function. Another technique is to define a square bounding box of predetermined size around one end point and to determine whether the other end point is within that bounding box. See FIG. 11B. We refer to this as the square distance function. A third technique is to define a square bounding box of predetermined size around one end point and then to rotate the bounding box around that end point to determine if at any rotational orientation the second end point falls within the bounding box. This will occur, if at all, when one corner of the bounding box lies on a line between the two end points. See FIG. 11C. We call this the Manhattan distance function.

56. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchida in view of Guo.

57. (d)-**"outputting the input circuit information which includes as, a wiring length, a Manhattan distance which is determined based on positions of part pins forming the target circuit and a wiring topology"** is disclosed by Guo at column 6 lines 35-49:

58. (e)-**"carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through the wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component".

59. (f)-**" carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through the wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform"** is disclosed by Tsuchida FIG 1 "simulation" and "expected operation" and "addition of noise reduction component".

60. MOTIVATION FOR CLAIMS 5 AND 6. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Guo to modify Tsuchida. One of ordinary skill in the art would have started with Tsuchida column 16 line 24 as disclosing an "allowable range" of voltage for the overshoot, and then looked to Guo for common techniques of characterizing distance between points. Note that Guo discloses three separate techniques for assessing distance, and that the first (radial distance) and third (Manhattan distance) techniques appear directly related by the square root of two. Specifically, the Manhattan distance equals the radial distance times the square root of two, where the Manhattan distance equals the full width of the bounding box.
61. Claims 13-15 are "apparatus" claims with the same limitations as "method" claims 4-6, and are rejected for the same reasons respectively.

Additional Cited Prior Art

62. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.
63. Koford US patent 6,493,658 column 43 line 32 discloses "manhattan distance" in the context of optimizing integrated circuit design. In the above 35 USC 103 rejections, the Guo patent was cited because Guo provides a clear definition of the term "manhattan distance", as well as other common distance assessing techniques.

Conclusion

64. All pending claims stand rejected.

Communication

65. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER